IDEC Chip Design Contest

A 101.6-dB-SNDR Fully Dynamic Zoom ADC Using A Closed-Loop Miller Compensated Floating Inverter Amplifier.

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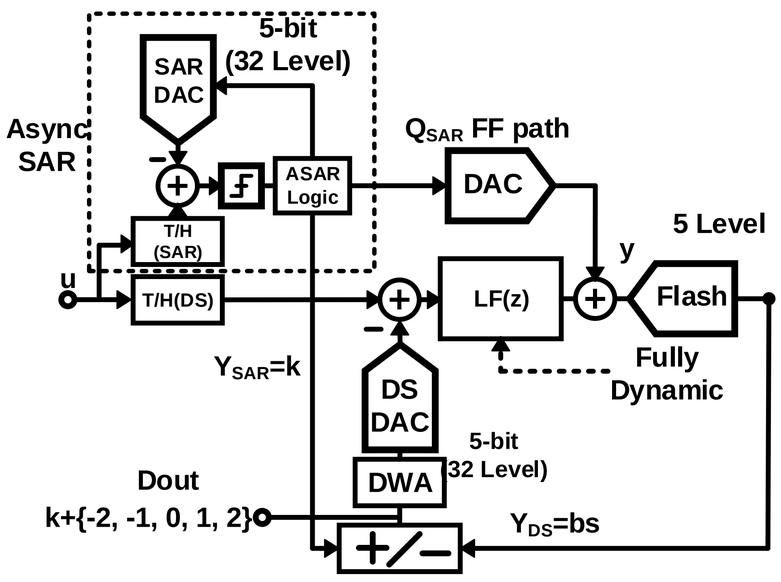
Introduction

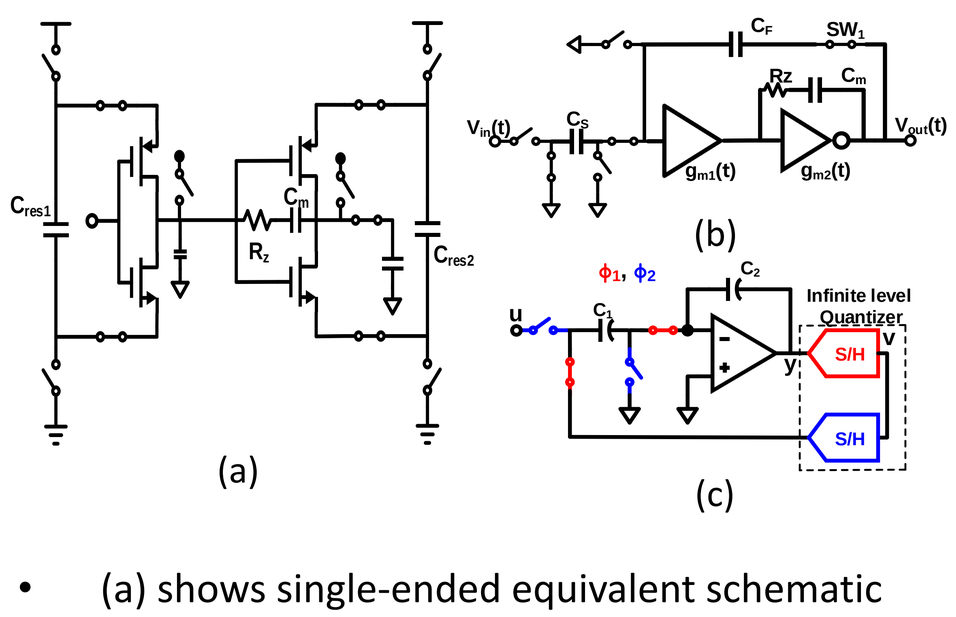
A floating inverter amplifier (FIA) is as an alternate circuit for the OTA in a switched-capacitor circuit [1]-[3]. There are two important factors for the above trend to occur. First, an FIA's self-quenching behavior makes system operate dynamically. Second, it is simple to embed the FIA to closed-loop system because of inherent common-mode feedback (CMFB), which is a tricky issue in dynamic amplifier or ring amplifier. A Miller-compensated 2-stage FIA is designed, then applied to a fully dynamic zoom ADC design. The prototype ADC a chieves 101.6 dB signal-to-noise and distortion ratio (SNDR) with an SNDR-based Schreier figure of merit (Fo M) of 174.2 dB at 2.56-MHz fs having linearly scalable bandwidth and power consumption as fs varies, as wel l as easy power duty-cycling.

Top block diagram



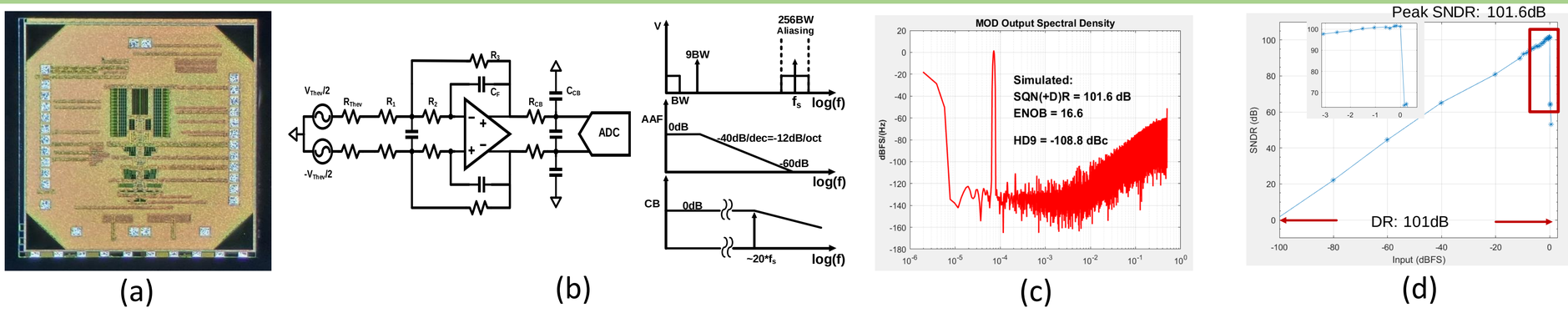
- A zoom ADC architecture is chosen to cope with limited output swing of FIA.
- Residue feed-forward path is realized to reduce quantization error leakage of SAR ADC [4].
- Over-ranging of 5 level quantizer provides 1.5 LSB redundancy to SAR ADC.

2-stage Miller compensated of FIA



- (a) shows single-ended equivalent schematic of the MC-FIA.
- (b) is a block-diagram of the proposed FIA-based switched-capacitor integrator.
- (c) illustrates simulation testbench to characterize gain and noise of time-variant system.

Measurement and Conclusion



- (a) shows a chip-photo. The prototype IC is implemented in a 0.18-μm CMOS process, and occupies 0.65 mm^2
- (b) depicts a block diagram of measurement setup. APx555 is used as a signal source. Analog front-end composed of anti-aliasing filter(2nd order MFB filter) and charge-bucket filter to cope with kickback.
- (c),(d) shows measured spectrum, and dynamic range along with the input.
- This research implements a fully-dynamic ADC with a SDNR>100 dB. There are no static component such as bias circuit or current sources. As a result, it achieves linearly scalable bandwidth and power consumption, as well as easy power duty-cycling

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

[1] M. Zhao et al., IEEE JSSC, vol. 57, pp. 709-718, Nov. 2021.
[2] X. Tang et al., ISSCC Dig. Tech. Papers, pp. 376-378, Feb. 2021.
[3] X.-Tang et al, IEEE JSSC, vol. 55 pp. 3248-3259, Sep. 2020.
[4] E.-Eland et al, IEEE JSSC, vol. 56 pp. 1207-1215, Apr. 2021.